International Journal of Electronics Engineering (ISSN: 0973-7383)
Volume 10 • Issue 2 pp. 720-725 June 2018-Dec 2018 www.csjournals.com

Newly Configured High Step-Up Chopper with Coupled Inductor and Voltage Doubler Circuits

[1]B.Muthuselvi
Asst.Prof, EEE Dept.,
M.I.E.T Engineering College, Tiruchirappalli

[2]Abirami.A
Asst.Prof, EEE Dept.,
M.I.E.T Engineering College, Tiruchirappalli

Abstract- A conventional dc-dc step up converter with coupled inductor provides moderate voltage gain but the disadvantage of conventional converter is high voltage stress on switches hence rating of the switch is high which increase the overall cost. In this paper a novel high step-up DC-DC converter with coupled-inductor and voltage-doubler circuit is proposed. This converter uses only two numbers of switches hence the complexity of control circuit is reduced. The converter achieves high step-up voltage gain with appropriate duty ratio and low voltage stress on the power switches. The energy stored in the leakage inductance of the coupled inductor can be recycled to the output. The operating principles of conventional and the proposed converters are analyzed and compared. The design procedure of the proposed converter is described. The control circuit required for proposed converter is implemented using a microcontroller circuit, reducing overall system cost and complexity.

This topology can be operated at frequencies (about 25 KHz), producing a very clean output spectrum. The output waveform is very clean with only the frequency (25kHz). The DC-DC converter with high step-up voltage gain is widely used for many applications, such as fuel-cell energy-conversion systems, solar-cell energy-conversion systems, and high-intensity-discharge lamp ballasts for automobile headlamps.

Keywords – Coupled-inductor, voltage-doubler, high step-up voltage gain.

I. INTRODUCTION

CONVENTIONAL BOOST CONVERTER WITH COUPLED INDUCTOR

A conventional high step-up DC-DC converter with coupled-inductor technique is shown in Fig. 2.2. The structure of this converter is very simple and the leakage-inductor energy of the coupled inductor can be recycled to the output. However, the voltage stresses on switch *S*1 and diode *D*1, which are equal to the output voltage, are high.

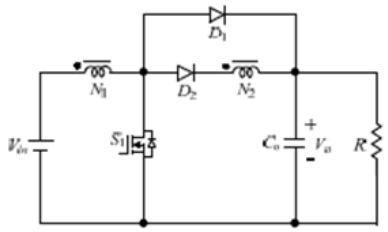

Fig 1 Circuit Configuration of the conventional high step DC-DC converter

Conventionally, the DC-DC boost converter is used for voltage step-up applications, and in this case this converter will be operated at extremely high duty ratio to achieve high step-up voltage gain. However, the voltage gain and the efficiency are limited due to the constraining effect of power switches, diodes, and the equivalent series resistance (ESR) of inductors and capacitors.

Merits and demerits of conventional high step-up DC-DC converter

MERITS
1. Simple structure
2. Recycling of the leakage-inductor energy of the coupled inductor to the output.

DEMERITS
1. Appearance of High voltage stresses, equal to output voltage on switch S1 and diode D1
2. Moderate voltage gain
3. Rating of switch & diode is high.

II. PROPOSED CONVERTER

A. Advancements in Proposed Converter

- High step-up voltage gain due to integrated coupled-inductor and voltage-doubler
- Energy efficient : Recycling of the leakage-inductor energy of the coupled inductor to the output.
- Reduced device voltage stresses ($V_o/2$)
- Selection of switches with low voltage rating and low ON-state resistance $R_{DS(ON)}$
- Double the voltage gain than that of the conventional high step-up converter
- The frequency of the magnetizing-inductor current for the proposed converter is double of

International Journal of Electronics Engineering (ISSN: 0973-7383)
Volume 10 • Issue 2 pp. 720-725 June 2018-Dec 2018 www.csjournals.com

the switching frequency. Thus, magnetizing-inductance of the coupled-inductor for the proposed converter can be designed to be less than the conventional high step-up converter under same switching frequency.

B. Block Diagram

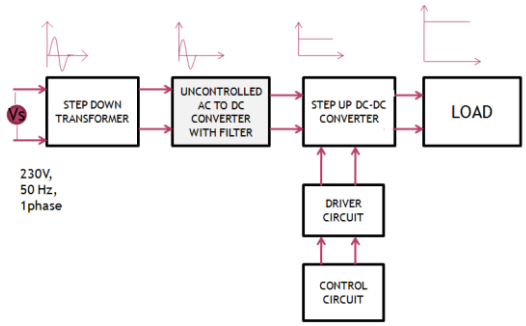

Fig 2 Block Diagram of Proposed converter

C. Circuit Configuration

A novel high step-up DC-DC converter, as shown in Fig. 3.2. The coupled-inductor and voltage-doubler techniques are integrated in the proposed converter to achieve high step-up voltage gain.

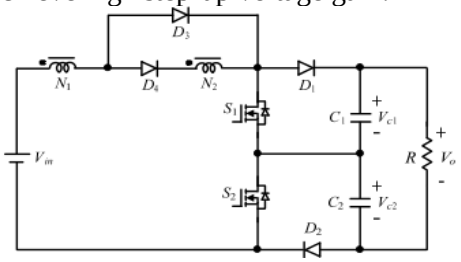

Fig 3 Circuit configuration of Proposed converter

The circuit configuration of the proposed converter, which consists of two active switches $S1$ and $S2$, one coupled inductor, four diodes $D1 – D4$, and two output capacitors $C1$ and $C2$. The simplified circuit model of the proposed converter is shown in Fig.3.5. The coupled inductor is modeled as a magnetizing inductor Lm, primary leakage inductor L_{k1}, secondary leakage inductor L_{k2}, and an ideal transformer. Capacitors C_{S1} and C_{S2} are the parasitic capacitor of S_1 and S_2. DC voltage doubler or voltage multiplier is a circuit which will increase some volts or double the voltage for example 3v to 5v, 6v to 12v or 12v to 24v, we can also call it as voltage booster circuit. A voltage doubler circuit consists of only two capacitors and two diodes. In order to simplify the circuit analysis of the proposed converter, some conditions are assumed as follows:

1) All components are ideal. ON-state resistance $R_{DS(ON)}$ of the active switches, the forward voltage drop of the diodes, and the equivalent series resistance (ESR) of the coupled-inductor and output capacitors are ignored.
2) Output capacitors C_1 and C_2 are sufficiently large, and the voltages across C_1 and C_2 are considered to be constant during one switching period.

C. Modes of Operation Power Stage

The operating principle is described as follows.

Mode I [t_0, t_1]:

At $t = t_0$, $S1$ and $S2$ are turned on. The current-flow path is shown in Fig. The DC-source energy is transferred to L_m and L_{k1} through $D3$, $S1$, and $S2$, so currents i_{Lm}, i_{Lk1}, and i_{D3} are increased. The energy stored in L_{k2} is released to L_m and L_{k1} through D_4, S_1, and S_2. Thus, i_{Lk2} is decreased. Meanwhile, the energy stored in L_{k2} is recycled. The energy stored in C_{S2} is rapidly and completely discharged. The energies stored in C_1 and C_2 are discharged to the load. This mode ends when i_{Lk2} is equal to zero at $t = t1$.

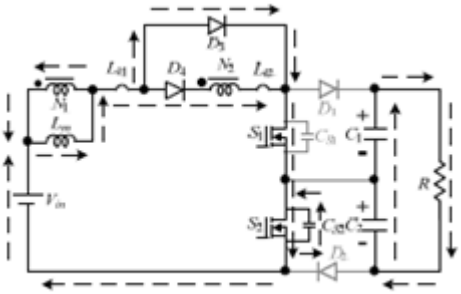

Fig 4 Mode I

Mode II [t_2, t_3]:

At $t = t_2$, S_1 is turned off and S_2 is still turned on. The current-flow path is shown in Fig. 5(c). The DC-source energy is still transferred to Lm, L_{k1}, and C_{S1}. Meanwhile, the voltage across S_1 is increased rapidly. The energies stored in C_1 and C_2 are still discharged to the load.

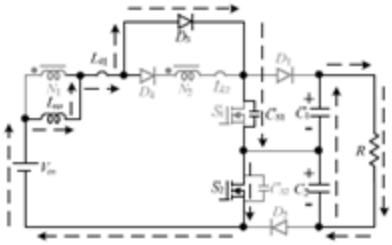

Fig 5 Mode II

Mode III [t_3, t_4]:

During this time interval, S_1 is still turned off and S_2 is still turned on. The current-flow path is shown in Fig.3.6 (d). The DC source, Lm, and L_{k1} are series-connected to transfer their energies to L_{k2}, C_1, and the load. Thus, i_{Lm} and i_{Lk1} are decreased and i_{Lk2} is increased. Meanwhile, the energy stored in $Lk1$ is

International Journal of Electronics Engineering (ISSN: 0973-7383)
Volume 10 • Issue 2 pp. 720-725 June 2018-Dec 2018 www.csjournals.com

recycled to C_1 and the load. The energy stored in C_2 is still discharged to the load. This mode ends when i_{Lk1} is equal to i_{Lk2} at $t = t_4$.

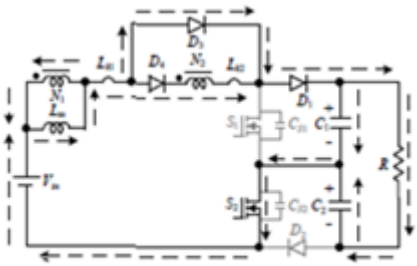

Fig 6 Mode III

Mode IV [t_5, t_6]:

At $t = t_5$, S_1 and S_2 are turned on. The current-flow path is shown in Fig.3.6 (f). The DC-source energy is transferred to L_m and L_{k1} through D_3, S_1, and S_2. So currents i_{Lm}, i_{Lk1}, and $iD3$ are increased. The energy stored in L_{k2} is released to L_m and L_{k1} through D_4, S_1, and S_2. Thus, i_{Lk2} is decreased. Meanwhile, the energy stored in L_{k2} is recycled. The energy stored in C_{S1} is rapidly and completely discharged. The energies stored in C_1 and C_2 are discharged to the load. This mode ends when i_{Lk2} is equal to zero at $t = t_6$.

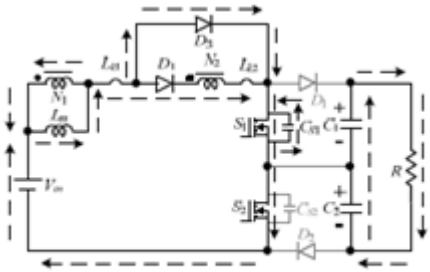

Fig 7 Mode IV

Mode V [t_7, t_8]:

At $t = t_7$, S_1 is still turned on and S_2 is turned off. The current-flow path is shown in Fig.3.6 (h). The DC-source is still transferred to L_m, L_{k1}, and C_{S2}. Meanwhile, the voltage across S_2 is increased rapidly. The energies stored in C_1 and C_2 are still discharged to the load.

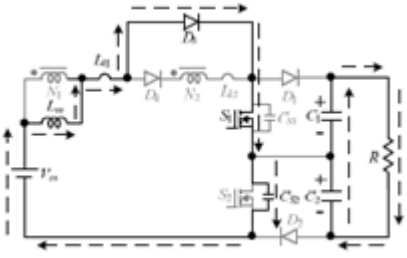

Fig 8 Mode V

Mode VI [t_8, t_9]:

During this period, S_1 is still turned on and S_2 is still turned off. The current-flow path is shown in Fig.3.6 (i). The DC source, L_m, and $Lk1$ are series-connected to transfer their energies to L_{k2}, C_2, and the load. Thus, i_{Lm} and i_{Lk1} are decreased and i_{Lk2} is increased. Meanwhile, the energy stored in L_{k1} is recycled to C_2 and the load. The energy stored in C_1 is still discharged to the load. This mode ends when i_{Lk1} is equal to i_{Lk2} at $t = t_9$. This mode ends when S_1 and S_2 are turned on at the beginning of the next switching period.

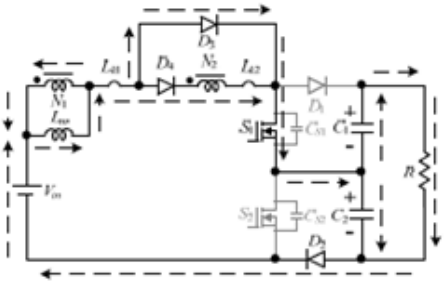

Fig 9 Mode VI

III DESIGN CALCULATION

1) *Duty Ratio*

$V_{in} = 12V$, $V_{out} = 100V$

$$\frac{Vo}{Vin} = \frac{1}{1-D}$$

$$\left(\frac{Vo}{Vin}\right) - \left(\frac{Vo}{Vin}\right) * D = 1$$

$$\frac{100}{12} - \left(\frac{100}{12}\right) * D = 1$$

$$D = 0.8799$$

2) *Select Inductance*

$$L > (1-D)^2 * D * \frac{R}{2} * F$$

$$> ((1-0.8799)^2 * 0.8799 * 160))/(2 * 25 * 10\text{^}3)$$

$$> 40.9\mu H \text{ Choosen } 47\mu H$$

Select Capacitances C_1 and C_2 :

$$Cmin > D * \frac{Vo}{Vr} * R * F$$

$$Cmin > 0.8799 * \frac{100}{10} * 160 * 25 * 10^3$$

$$Cmin > 22\mu H$$

$$C1 = 47\mu H \ \& \ C2 = 47\mu H$$

$$Cmin = \frac{C1 * C2}{(C1 + C2)}$$

$$Cmin = \frac{47 * 47}{47 + 47} = 23.5\mu f > Cmin$$

$$Choose\ C1\&C2 = 47\mu f$$

International Journal of Electronics Engineering (ISSN: 0973-7383)
Volume 10 • Issue 2 pp. 720-725 June 2018-Dec 2018 www.csjournals.com

IV SIMULATED RESULTS

A. CONVENTIONAL CONVERTER

It includes the step-up converter with a single switch. The simulation circuit for the conventional method is shown in fig

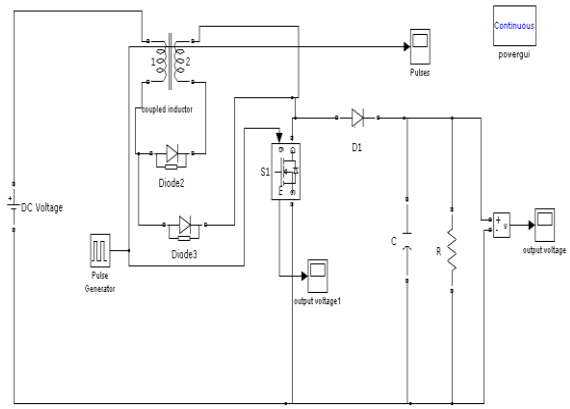

Fig 13 Conventional step-up converter with one switch

1. *Input and Output Voltage*

The input and output voltage is shown in fig 14.For a input voltage of 12V DC, the conventional converter produce 50V DC output

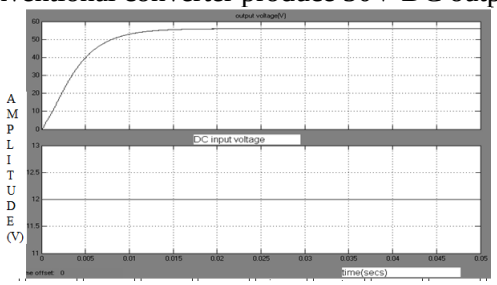

Fig 14 Input and Output Voltage

2. *Voltage stress across switch*

The simulation of the voltage across MOSFET is shown in fig 15. Switch is stressed with 50V DC which is equal to output voltage.

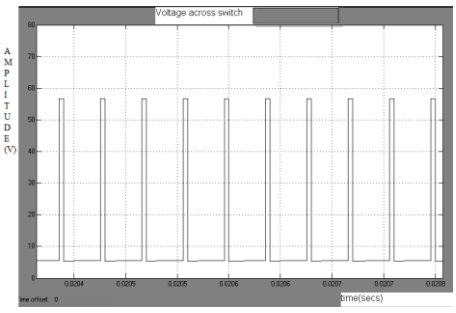

Fig 15 MOSFET Voltage

B.PROPOSED CONVERTER – OPEN LOOP

It includes the step-up converter with a two switches. The simulation circuit for the conventional method is shown in fig

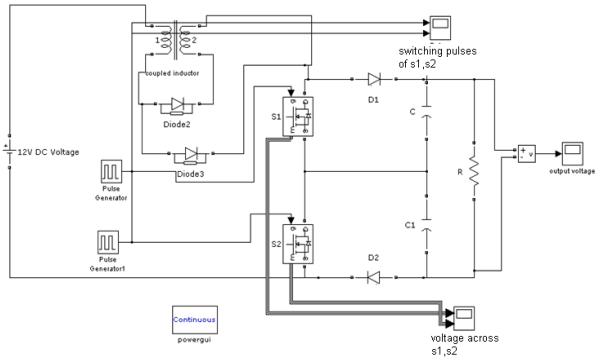

Fig 16 Proposed step-up converter with two switch

1. *Output Voltage*

The simulation of the output voltage is shown in fig 17. For a input voltage of 12V DC, the proposed converter produce 100V DC output

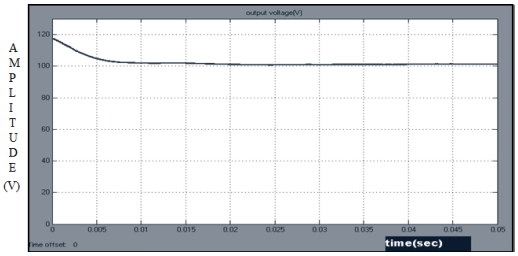

Fig 17 Output Voltage

2.Voltage across the switches

The simulation of the voltage across MOSFET is shown in fig.18. Switch is stressed with 50V DC which is equal to half the output voltage

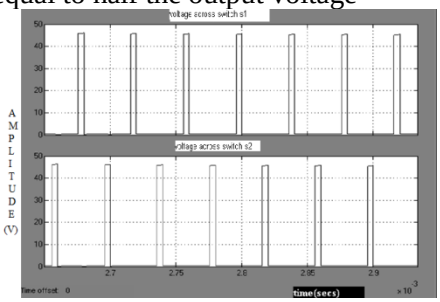

Fig 18 MOSFET 1& 2 Voltage

C.PROPOSED CONVERTER – CLOSED LOOP

It includes proposed converter with closed loop as shown in fig 19

International Journal of Electronics Engineering (ISSN: 0973-7383)
Volume 10 • Issue 2 pp. 720-725 June 2018-Dec 2018 www.csjournals.com

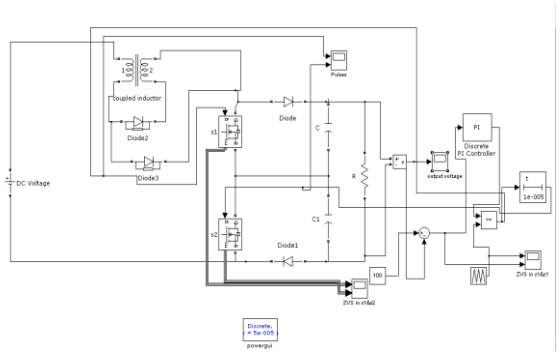

Fig 19 Proposed converter with closed loop

1. *Output Voltage*

The simulation of the output voltage is shown in fig 20. For a input voltage of 12V DC, the proposed converter with closed loop produce 100V DC output

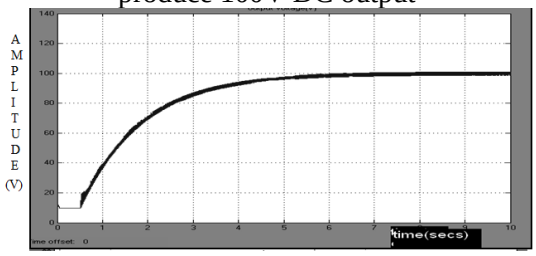

Fig 20 Output Voltage

2.Voltage across the switches

The simulation of the voltage across MOSFET is shown in fig.21. Switch is stressed with 50V DC which is equal to half the output voltage

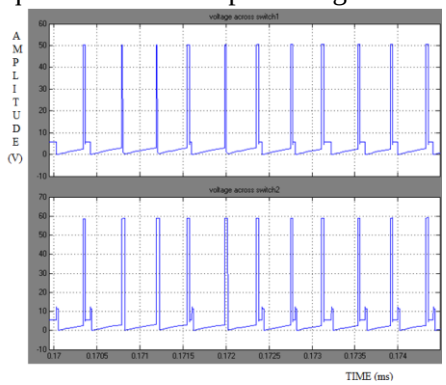

Fig 21 MOSFET 1& 2 Voltage

D.PROPOSED CONVERTER WITH MOTOR LOAD– OPEN LOOP

It includes proposed converter with motor load as shown in fig 22

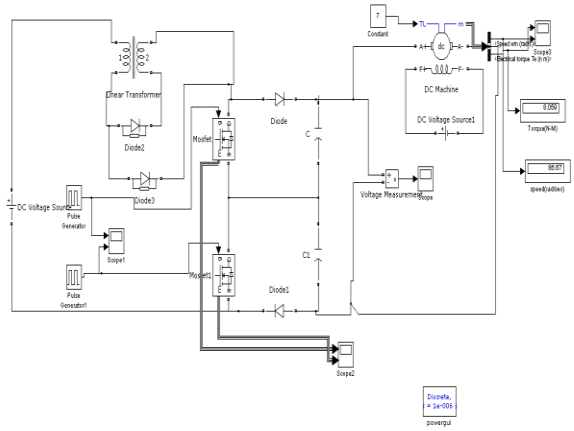

Fig 22 Proposed converter with motor load

1. *Output voltage*

The simulation of the output voltage is shown in fig 23. For a input voltage of 12V DC, the proposed converter with motor load produce 100V DC output.

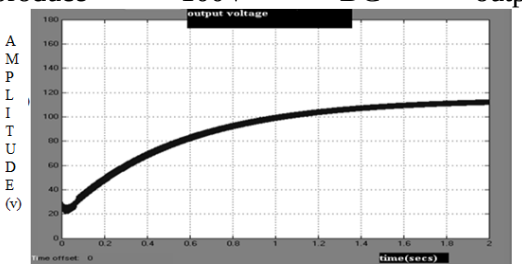

Fig 23 Output voltage

2. *Speed and Torque*

Fig 24 shows speed & torque of for the input voltage of 12V DC and output of 100V DC

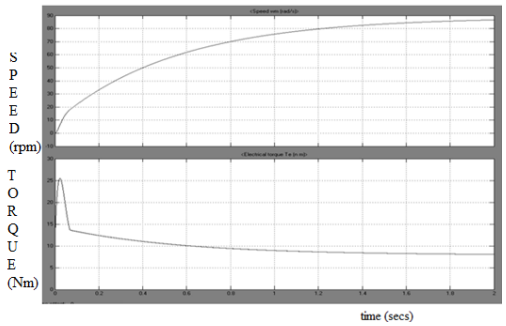

Fig 24 Speed & Torque

E.COMPARISON

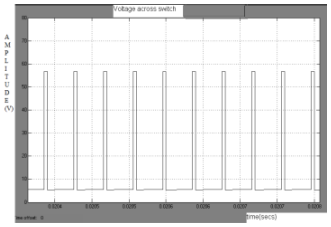

Fig a Voltage across the switch in conventional converter

International Journal of Electronics Engineering (ISSN: 0973-7383)
Volume 10 • Issue 2 pp. 720-725 June 2018-Dec 2018 www.csjournals.com

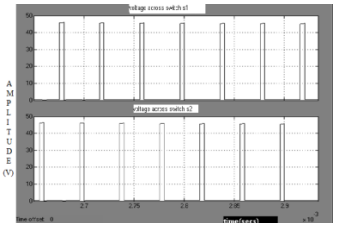

Fig b Voltage across the switch in proposed converter

With reference to the figures, it is observed that the voltage stress across switch

Table: 1 Variation of Output voltage with Duty ratio

From the table, it is observed that by varying the duty ratio, the output voltage is varied.

S.No.	Duty Ratio (%)	Output Voltage (volts)
1.	70	50
2.	75	61
3.	80	73
4.	85	82
5.	89	100

Table: 2 Variation of Output voltage with Duty ratio

From the table, it is observed that by varying the duty ratio, the speed and torque of the motor is varied.

S.No.	Duty Ratio (%)	Speed (rps)	Torque(Nm)
1.	70	49.75	7.498
2.	75	58	7.59
3.	80	68.38	7.68
4.	85	80.94	7.816
5.	89	86.69	8.08

V CONCLUSION

Novel high step-up DC-DC converter is presented in this paper. The coupled-inductor and voltage-doubler circuits are integrated in the proposed converter to achieve high step-up voltage gain. The energy stored in the leakage inductor of the coupled inductor is recycled. The voltages across the switches are half the level of the output voltage during the steady state period.

- The performance of conventional step-up converter and the proposed converter are compared and analysed.
- The proposed converter is simulated with MATLAB SIMULINK TOOL model for both open loop and closed loop conditions with motor load and results are presented.
- For various duty ratios, the output voltage of the proposed converter hence speed and torque of the motor load are varied and the results were presented.

VI REFERENCES

[1] L. Huber and M. M. Jovanovic, "A design approach for server power supplies for networking applications," *Proc. IEEE APEC*, pp. 1163-1169, 2000.

[2] L. H. Barreto, E. A. Coelhp, V. J. Farias, J. C. Oliveira, L. C. Freitas, and J. B. Vieira, "A quasi-resonant quadratic boost converter using a single resonant network," *IEEE Trans. Ind. Electron.*, vol. 52, no. 2, pp. 552-557, Apr. 2005.

[3] L. S. Yang, T. J. Liang, and J. F. Chen, "Transformerless DC-DC converters with high step-up voltage gain," *IEEE Trans. on IndustrialV Electronics*, vol. 56, no.8, pp. 3144-3152, Aug. 2009.

[4] O. Abutbul, A. Gherlitz, Y. Berkovich, and Ioinovici, "Step-up switching-mode converter with high voltage gain using a switched-capacitor circuit," *IEEE Trans. Syst. I, Fundam. Theory Appl.*,vol. 50, no. 8, pp. 1098-1102, Aug. 2003.

[5] N. P. Papanikolaou and E. C. Tatakis, "Active voltage clamp in flyback converters operating in CCM mode under wide load variation," *IEEE Trans.Ind. Electron.*, vol. 51, no. 3, pp.632–640, Jun. 2004.